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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,234	03/16/2004	Fu-Hsin Chen	24061.79	2028

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/801,234	CHEN ET AL.
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 24-28* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 12-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,9,24,25 and 28* is/are rejected.

7)☒ Claim(s) *10,11,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 08/19/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8,9,24,25, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by HOSHINO ET AL. (2001/0012671).

With regard to claims 8 and 9 Hoshino et al. discloses a high-voltage MOS transistor comprising a substrate 1; a gate structure composed of a gate 7, a gate dielectric layer 6, and a gate spacer (the unnumbered cross-hatched region seen beside the unnumbered gate in figure 14a) overlying the substrate 1, the gate structure having a first side and a second side opposite to the first side; a first doping region 8 (Hoshino et al. call this the "offset region," as is common practice) with a first dosage formed in the substrate 1 on the first side of the gate structure and partially covered by the gate structure; a drain region (a second doping region 9 with a second dosage formed within the first doping region 8) adjacent to the edge on the first side of the gate structure; a source region (a third doping region 10 with the second dosage formed in the substrate

1) adjacent to the edge of the second side of the gate structure; and a channel region 5 formed in the substrate 1 between the first 8 and third 10 doping regions by turning on the high-voltage MOS transistor to pass current between the source 10 and drain 9 regions. Note figures 1, 14A and paragraphs 0135-0140 and 0211 of Hoshino et al.

Applicants are asked to next direct their attention to figures 32 and 36, and paragraphs 0256 and 0259 of Hoshino et al. In figure 32 Hoshino et al. show the on resistance increasing linearly with increasing gate (gate length being proportional to channel length) length. The slope of Hoshino et al.'s plot of on resistance versus gate length defines a resistance per unit length of Hoshino et al.'s channel region. In figure 36 Hoshino et al. show the on resistance increasing linearly with increasing offset region (Hoshino et al.'s "first doping region") length. The slope of Hoshino et al.'s plot of on resistance versus offset length defines a resistance per unit length of Hoshino et al.'s first doping region. Note that the two slopes are substantially equal. Hoshino et al. thus discloses that a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

With regard to claims 24 and 25 Hoshino et al. discloses a high-voltage MOS transistor comprising a first drain region 8 with a first dosage formed in a substrate 1, wherein the first drain region 8 extends horizontally from a first point proximate to an upper surface of the substrate 1 to a second point proximate to the upper surface; a gate structure 7 overlying the substrate 1 and covering a portion of the first drain region 8 extending from the first point to a third point of the first drain region 8 located between

the first and second points; a spacer (the unnumbered cross-hatched region seen beside the unnumbered gate in figure 14a) in contact with the gate structure 7 and covering a portion of the first drain region 8 from the third point to a fourth point of the first drain region 8 located between the third and second points; a second drain region 9 with a second dosage formed within the first drain region 8, wherein the second drain region 9 extends substantially from the fourth point to a fifth point of the first drain region 8 located between the fourth and second points, and wherein the portion of the first drain region 8 extending from the fifth point to the second point is at substantially the same horizontal level in the substrate 1 as the first point; and a source region 10 formed in the substrate 1 on the opposite side of the gate structure 7 from the first drain region 8, wherein a channel region 5 formed in the substrate 1 between the first drain region 8 and source region 10 has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region 8, and a field oxide layer 21 (seen, albeit without part #, in figure 14B substantially abutting the first doped region at the second point – seen, with part #, in figure 9B). Note figures 1, 9B, 14A, 14B and paragraphs 0135-0140 and 0211 of Hoshino et al.

Applicants are asked to next direct their attention to figures 32 and 36, and paragraphs 0256 and 0259 of Hoshino et al. In figure 32 Hoshino et al. show the on resistance increasing linearly with increasing gate (gate length being proportional to channel length) length. The slope of Hoshino et al.'s plot of on resistance versus gate length defines a resistance per unit length of Hoshino et al.'s channel region. In figure

36 Hoshino et al. show the on resistance increasing linearly with increasing offset region (Hoshino et al.'s "first doping region") length. The slope of Hoshino et al.'s plot of on resistance versus offset length defines a resistance per unit length of Hoshino et al.'s first doping region. Note that the two slopes are substantially equal. Hoshino et al. thus discloses that a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

With regard to claim 28 Hoshino et al. discloses a high-voltage MOS transistor comprising a first drain region 8 formed in a substrate 1; a gate structure 7 overlying the substrate 1 and covering a first portion of the first drain region 8; a spacer (the unnumbered cross-hatched region seen beside the unnumbered gate in figure 14a) in contact with the gate structure 7 and covering a second portion of the first drain region 8 adjacent to the first portion; a second drain region 9 formed within the first drain region 8, wherein the second drain region 9 extends substantially from the second portion in the direction opposite the gate structure 7 and spacer, wherein the portion of the first drain region 8 extending beyond the second drain region 9 is at substantially the same horizontal level in the substrate 1 as the first portion; and a source region 10 formed in the substrate 1 on the opposite side of the gate structure 7 from the first drain region 8, wherein a channel region 5 formed in the substrate 1 between the first drain region 8 and source region 10 has a resistance per unit length that is substantially equal to a resistance per unit length of the first drain region 8. Note figures 1 and 14A and paragraphs 0135-0140 and 0211 of Hoshino et al.

Applicants are asked to next direct their attention to figures 32 and 36, and paragraphs 0256 and 0259 of Hoshino et al. In figure 32 Hoshino et al. show the on resistance increasing linearly with increasing gate (gate length being proportional to channel length) length. The slope of Hoshino et al.'s plot of on resistance versus gate length defines a resistance per unit length of Hoshino et al.'s channel region. In figure 36 Hoshino et al. show the on resistance increasing linearly with increasing offset region (Hoshino et al.'s "first doping region") length. The slope of Hoshino et al.'s plot of on resistance versus offset length defines a resistance per unit length of Hoshino et al.'s first doping region. Note that the two slopes are substantially equal. Hoshino et al. thus discloses that a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region.

Response to Arguments

3. Applicant's arguments filed 08/19/05 have been fully considered but they are not persuasive.

It is argued, at page 8 and again on page 9 of the remarks, that "As described above, the cited figures and text of Hoshino fail to teach or suggest [that a resistance per unit length of the channel region is substantially equal to a resistance per unit length of the first doping region]" because, by applicant's calculation, the resistance per unit length of Hoshino et al.'s channel region is 2.75 in arbitrary units, while the resistance

per unit length of Hoshino et al.'s first doping region in the same units is 2.1. 2.75, in applicant's view, is not "substantially equal" to 2.1.

The Federal Circuit was recently asked, in Playtex Products Inc. v. Procter & Gamble Co, to construe the claim term "substantially" The court held:

> "The term 'substantial' is a meaningful modifier implying 'approximate,' rather than 'perfect.'" Liquid Dynamics, 355 F.3d at 1368. But the definition of "substantially flattened surfaces" adopted by the district court introduces a numerical tolerance to the flatness of the gripping area surfaces of the claimed applicator. That reading contradicts the recent precedent of this court, interpreting such terms of degree. In Cordis Corp. v. Medtronic AVE, Inc., 339 F.3d 1352, 1361 [67 USPQ2d 1876] (Fed. Cir. 2003), we refused to impose a precise numeric constraint on the term "substantially uniform thickness," noting that the proper interpretation of this term was "of largely or approximately uniform thickness" unless something in the prosecution history imposed the "clear and unmistakable disclaimer" needed for narrowing beyond this plain-language interpretation. Id. Moreover, in Anchor Wall Sys. v. Rockwood Retaining Walls, Inc., 340 F.3d 1298 [67 USPQ2d 1865] (Fed. Cir. 2003), we held that "the phrase 'generally parallel' envisions some amount of deviation from exactly parallel," and that "words of approximation, such as 'generally' and 'substantially,' are descriptive terms 'commonly used in patent claims to avoid a strict numerical boundary to the specified parameter.'" Id. at 1311. In support of this holding, we noted that "nothing in the prosecution history [of the Anchor Wall patent]. clearly limit[ed] the scope of 'generally parallel' such that the adverb 'generally' does not broaden the meaning of parallel." Id. Similarly, in this case we find that in claiming, "substantially flattened surfaces," Playtex claimed more than flat surfaces.

Playtex Products Inc. v. Procter & Gamble Co., 73 USPQ2d 2010, 2015 (Fed.Cir 3/7/2005). The last sentence bears repeating, as it appears to hold the key to this holding: "[I]n claiming, 'substantially flattened surfaces,' Playtex claimed more [emphasis added] than flat surfaces." In other words, the word "substantially," as a modifier, broadens (claims more than) the modified term. In *Playtex,* the result was that a substantially flattened surface was in fact a round surface that approximated, but did not reach, flatness. Further, it was error, in the court's view, to construe "substantially flattened surfaces" as requiring the introduction of a numerical tolerance, or to construe such a term as imposing precise numeric constraints.

Construing "substantially equal resistances per unit length" to mean "largely or approximately the same resistances per unit length" (in keeping with *Cordis Corp. v. Medtronic AVE, Inc.,* 339 F.3d 1352, 1361, as cited by the *Playtex* court), it seems clear that when comparing resistances (which often vary by orders of magnitude), 2.75 (as calculated by applicant) is in fact "substantially equal" to 2.1.

Allowable Subject Matter

4. Claims 10,11,26, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
09/05